IN THE CLAIMS:

Please amend claims 1, 8, and 16 as follows. Please cancel claim 2 without prejudice or disclaimer. Please add new claims 17-19.

1. (Currently Amended) An interleaving method for performing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said method comprising the steps of:

a) storing data samples in a memory array comprising a plurality of memory devices;

b) using a first portion of an address of said memory array to address said memory devices;

c) using a second portion of said address to select at least one memory device to be accessed; ~~and~~

d) changing a position of said first portion and said second portion within said address, when an access order is changed between a linear order and an interleaved order; and

e) performing a parallel access in a multiplexed manner using said second portion of said address portion as a multiplexing index.

2. (Canceled).

3. (Previously Presented) A method according to claim 1, wherein said second portion of said address corresponds to a predetermined number of most significant bits of said address during a linear access order, and corresponds to a predetermined number of least significant bits of said address during an interleaved access order.

4. (Previously Presented) A method according to claim 3, wherein said first portion of said address corresponds to a remaining number of bits within said address.

5. (Previously Presented) A method according to claim 1, further comprising the step of subjecting said first portion of said address to an interleaving processing during an interleaved access order.

6. (Previously Presented) A method according to claim 1, wherein said first portion of said address comprises ten address bits and said second portion of said address comprises two address bits.

7. (Previously Presented) A method according to claim 1, further comprising the step of generating said first portion of said address by an address counting function.

8. (Currently Amended) An interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said interleaving apparatus comprising:

a) a memory array with a plurality of memory devices for storing data samples;

b) addressing means for addressing said memory devices by applying a first portion of an address to said memory devices and by using a second portion of said address to select at least one memory device to be accessed; ~~and~~

c) change means for changing a position of said first portion and said second portion within said address in response to a change between a linear order and interleaved order; and

d) means for performing a parallel access in a multiplexed manner using said second portion of said address portion as a multiplexing index.

9. (Previously Presented) An apparatus according to claim 8, wherein said memory devices are single-port RAM devices.

10. (Previously Presented) An apparatus according to claim 8, wherein said interleaving apparatus is integrated on a single chip device.

11. (Previously Presented) An apparatus according to claim 8, wherein said addressing means comprises an address counter for generating said first address.

12. (Previously Presented) An apparatus according to claim 11, further comprising interleaving means for converting an output address of said address counter according to a predetermined interleaving scheme to generate said first portion of said address during an interleaved access order.

13. (Previously Presented) An apparatus according to claim 12, wherein said interleaving means comprises at least one of an address translation table and an address logic.

14. (Previously Presented) An apparatus according to claim 8, wherein said change means comprises a control switch for receiving said address and for switching said first portion and second portion within said address to respective output parts in response to an access order selection signal.

15. (Previously Presented) An apparatus according to claim 8, wherein said interleaving apparatus comprises a turbo interleaver for use in a turbo decoder.

16. (Currently Amended) An interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said interleaving apparatus comprising:

a) a memory array with a plurality of memory devices for storing data samples;

b) an addresser configured to address said memory devices by applying a first portion of an address to said memory device and by using a second portion of said address to select at least one memory device to be accessed; ~~and~~

c) a changer configured to change a position of said first portion and said second portion within said address in response to a change between a linear order and an interleaved order; and

d) an access provider configured to provide a parallel access in a multiplexed manner using said second portion of said address portion as a multiplexing index.

17. (New) An interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said interleaving apparatus comprising:

a) a memory array with a plurality of memory devices for strong data samples;

b) addressing means for addressing said memory devices by applying a first portion of an address to said memory devices and by using a second portion of said address to select at least one memory device to be accessed, wherein said addressing means comprises an address counter for generating said first address;

c) change means for changing a position of said first portion and said second portion within said address in response to a change between a linear order and interleaved order; and

d) interleaving means for converting an output address of said address counter according to a predetermined interleaving scheme to generate said first portion of said address during an interleaved access order.

18. (New) An apparatus according to claim 17, wherein said interleaving means comprises at least one of an address translation table and an address logic.

19. (New) An interleaving apparatus for providing parallel access in a linear and interleaved order to a predetermined number of stored data samples, said interleaving apparatus comprising:

a) a memory array with a plurality of memory devices for storing data samples;

b) addressing means for addressing said memory devices by applying a first portion of an address to said memory devices and by using a second portion of said address to select at least one memory device to be accessed, wherein said addressing means comprises an address counter for generating said first address;

c) change means for changing a position of said first portion and said second portion within said address in response to a change between a linear order and interleaved order, wherein said change means comprises a control switch for receiving said address and for switching said first portion and second portion within said address to respective output parts in response to an access order selection signal.